EVM3864-PQ-00A

7V, 6A, Step-Down Power Module Evaluation Board

DESCRIPTION

The EVM3864-PQ-00A is an evaluation board designed to demonstrate the capabilities of the MPM3864, a fully integrated, synchronous rectified, step-down, DC/DC power module with up to 6A of continuous current.

The MPM3864 adopts constant-on-time (COT) control to provide fast transient response, easy loop design, and tight output regulation. Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

It is recommended to read the MPM3864 datasheet prior to making any changes to the EVM3864-PQ-00A.

PERFORMANCE SUMMARY (1)

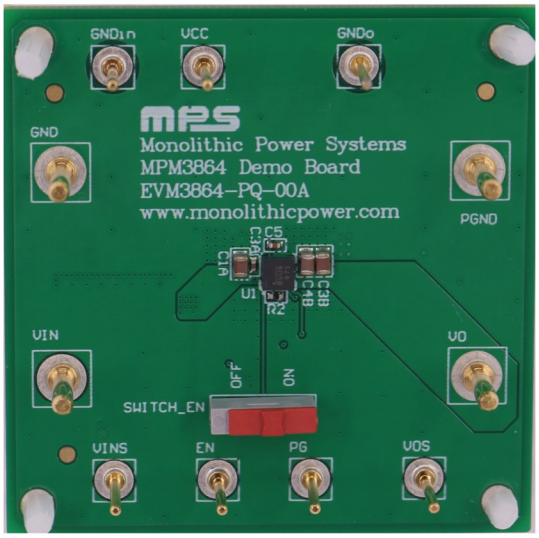
Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		2.75V to 7V
Output voltage (V_{OUT})	Default configuration	1.2V
Maximum output current (I_{OUT})	V_{IN} = 2.75V to 7V	6A
Typical efficiency	V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A, f_{SW} = 1.2MHz	83.4%
Peak efficiency	V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A, f_{SW} = 1.2MHz	89.7%
Switching frequency (f_{SW})	Default configuration	1.2MHz

Note:

1) For different V_{IN} and V_{OUT} specifications with different output capacitors, the application circuit parameters may require changes.

EVALUATION BOARD



LxWxH (5.1cmx5.1cmx1.6cm)

Board Number	MPS IC Number
EVM3864-PQ-00A	MPM3864GPQ

QUICK START GUIDE

The EVM3864-PQ-00A evaluation board is easy to set up and use to evaluate the performance of the MPM3864. For proper measurement equipment set-up, refer to Figure 1 and follow the steps below:

1. Preset the power supply (V_{IN}) between 2.75V and 7V, then turn off the power supply. (2)
2. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
3. Connect the load terminals to: (3)
   a. Positive (+): VOUT
   b. Negative (-): GND
4. After making the connections, turn on the power supply. The board should automatically start up.
5. Check for the proper output voltage (V_{OUT}) between the VOUTSENSE and GNDSENSE terminals.
6. Once the proper V_{OUT} is established, adjust the load within the operating range, then measure the efficiency, output ripple voltage, and other parameters. (3)

Notes:

2) Ensure that V_{IN} does not exceed 7V.
3) There is no initial load by default.
4) When measuring the output voltage ripple or input voltage ripple, do not use the oscilloscope probe's long ground lead.

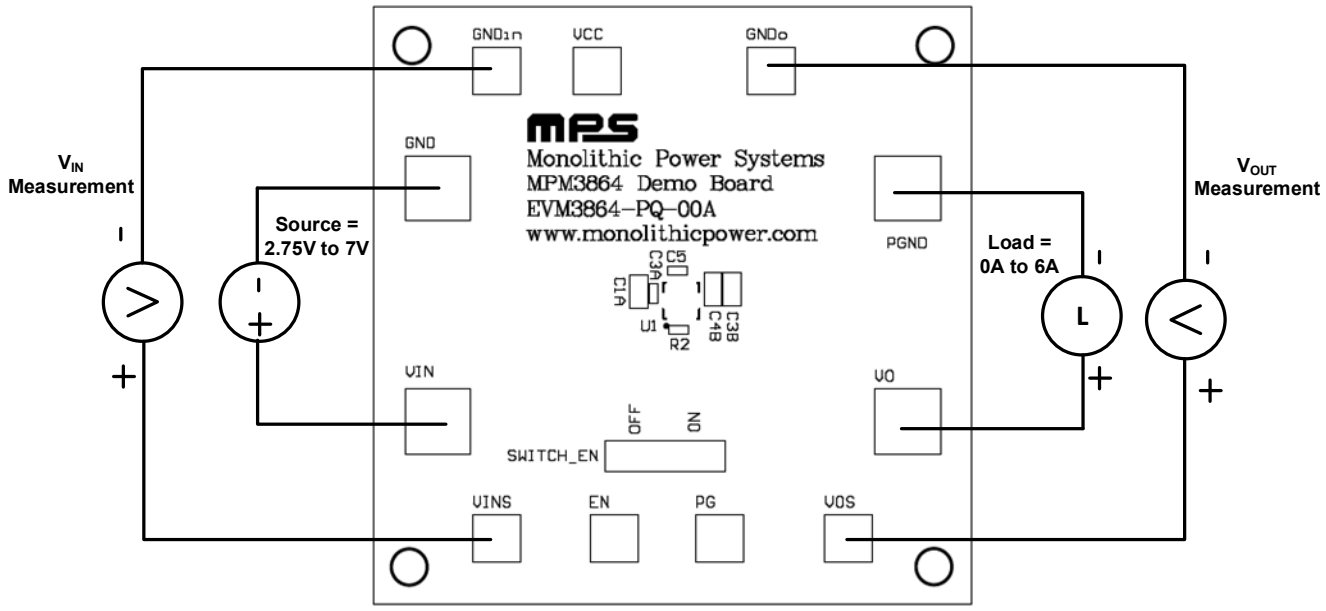


Figure 1: Proper Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

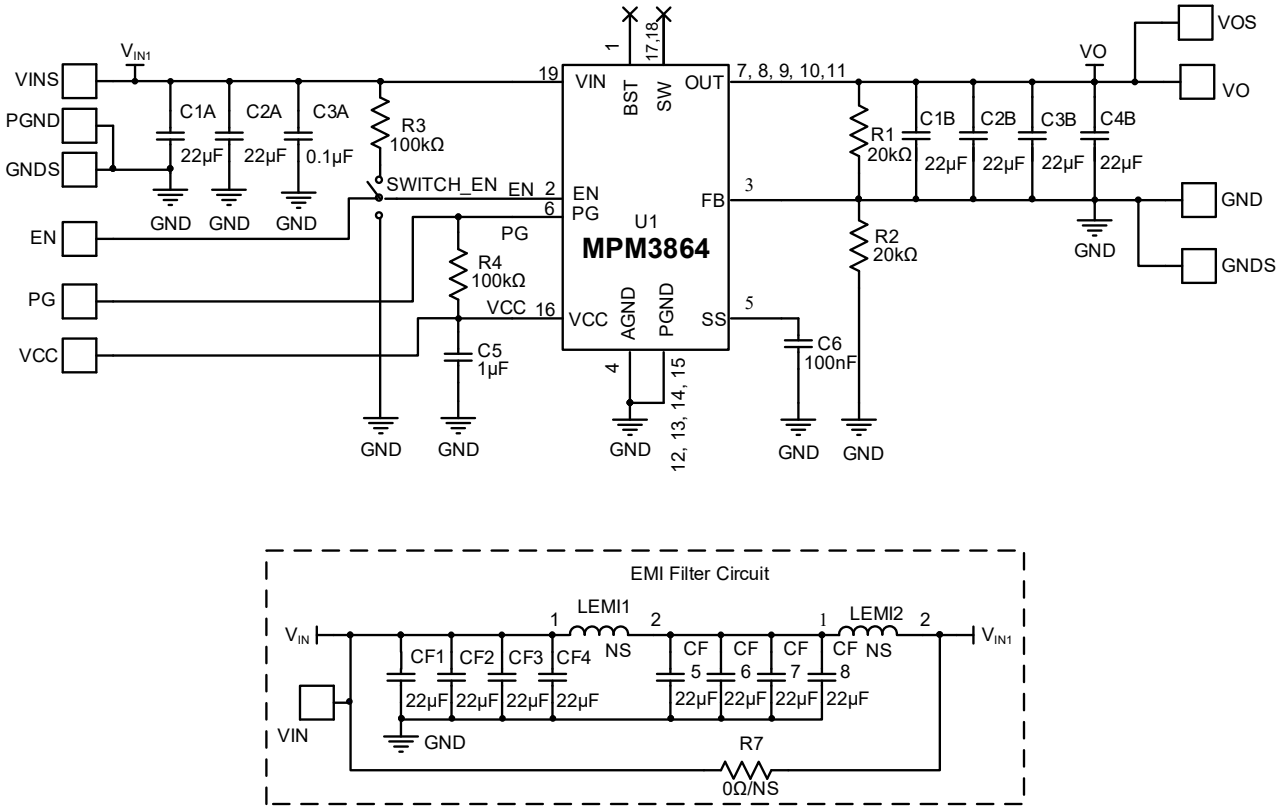


Figure 2: Evaluation Board Schematic

EVM3864-PQ-00A BILL OF MATERIALS

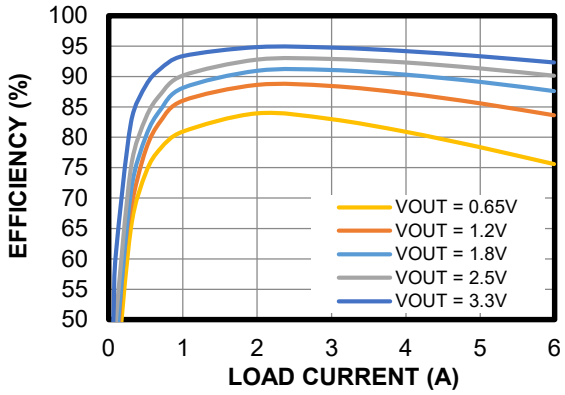
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
6	C1A, C1B, C2A, C2B, C3B, C4B	22µF	Ceramic capacitor, 25V	0805	Murata	GRM21BD71A226ME44L
2	C3A, C6	0.1µF	Ceramic capacitor, 25V	0402	Murata	GRM155R71C104KA88D
1	C5	1µF	Ceramic capacitor, 6.3V	0402	Wurth	885012206026
0	CF1, CF2, CF3, CF4, CF5, CF6, CF7, CF8, LEMI1, LEMI2	NS				
7	EN, GNDS, GNDS, PG, VINS, VOS, VCC	Φ1	Copper pin	DIP	Any	
4	GND, GND, VO, VIN	Φ2	Copper pin	DIP	Any	
2	R1, R2	20kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-0720KL
2	R3, R4	100kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-07100KL
1	R7	0Ω	Film resistor, 1%	2512	Yageo	RC2512FK-070RL
1	SWITCH_EN	500mA	Switch slide SPDT, 5V	10mmx 2.5mm	Wurth	450301014042
1	U1	MPM3864	1.2MHz, synchronous, rectified, 6A, step-down power module	ECLGA (3mmx3mm)	MPS	MPM3864GPQ

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

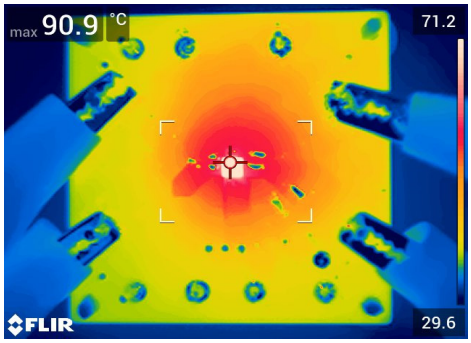
Efficiency vs. Load Current

V_{IN} = 5V



Thermal Rise

I_{OUT} = 6A, T_A = 29.6°C

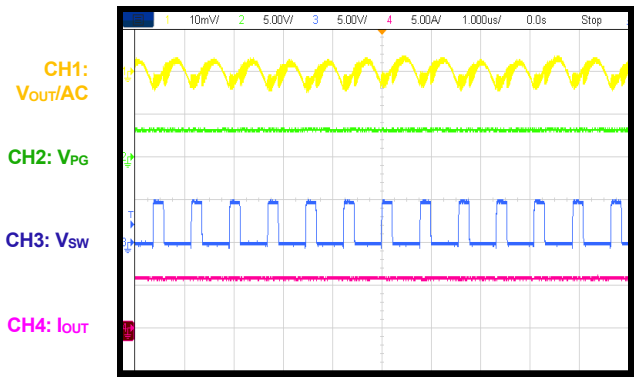


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

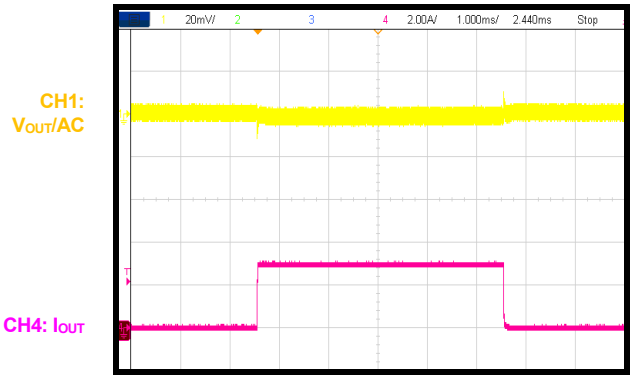
Steady State and Output Ripple

I_{OUT} = 6A



Load Transient Output Ripple

I_{OUT} = 0A to 3A, slew rate = 2.5A/µs



PCB LAYOUT

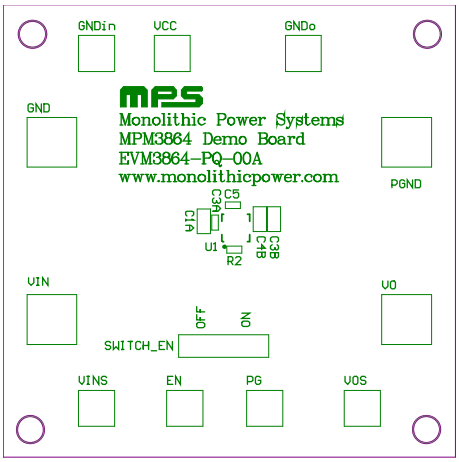


Figure 3: Top Silk

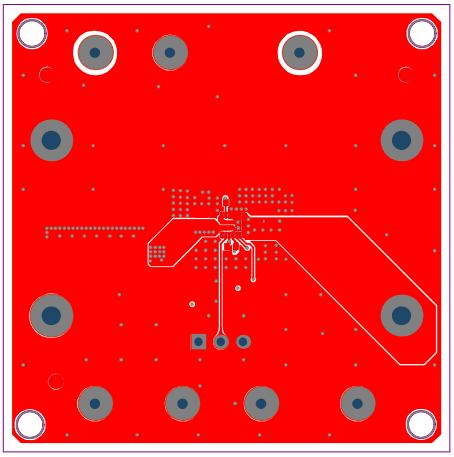


Figure 4: Top Layer

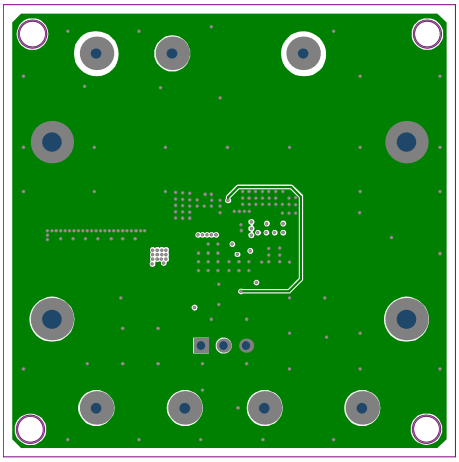


Figure 5: Mid-Layer 1

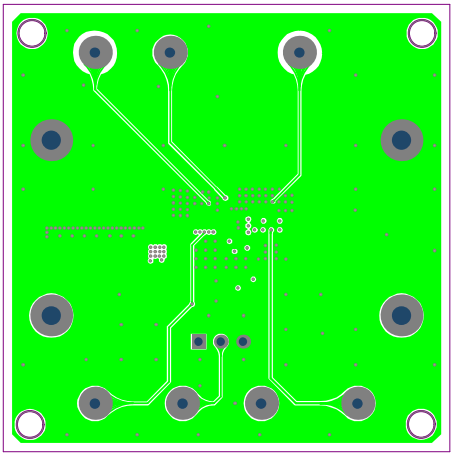


Figure 6: Mid-Layer 2

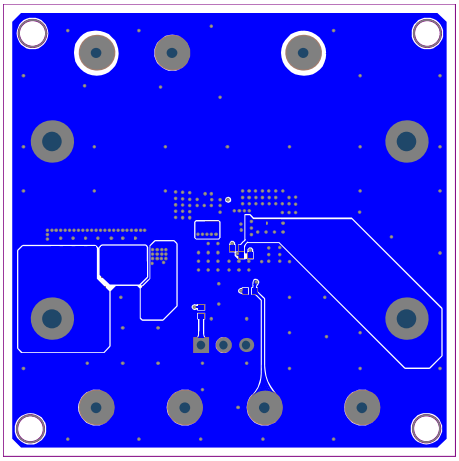


Figure 7: Bottom Layer

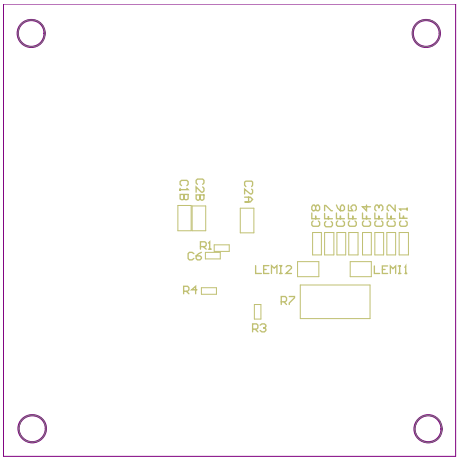


Figure 8: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/13/2021	Initial Release	-